

UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
XA-9375

Total Pages in this Submission

TO THE ASSISTANT COMMISSIONER FOR PATENTS

Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

CACHE MEMORY ALLOCATION METHOD

and invented by:

Kazuo Aisaka
Keisuke Toyama

jc825 U.S. PTO
09/688360
10/12/00

If a **CONTINUATION APPLICATION**, check appropriate box and supply the requisite information:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No. _____

Which is a:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: _____

Which is a:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: _____

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 56 pages and including the following:
 - a. ☒ Descriptive Title of the Invention
 - b. ☐ Cross References to Related Applications (if applicable)
 - c. ☐ Statement Regarding Federally-sponsored Research/Development (if applicable)
 - d. ☐ Reference to Microfiche Appendix (if applicable)
 - e. ☒ Background of the Invention
 - f. ☒ Brief Summary of the Invention
 - g. ☒ Brief Description of the Drawings (if drawings filed)
 - h. ☒ Detailed Description
 - i. ☒ Claim(s) as Classified Below
 - j. ☒ Abstract of the Disclosure

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Application Elements (Continued)

3. ☒ Drawing(s) (when necessary as prescribed by 35 USC 113)
- a. ☒ Formal Number of Sheets 13
- b. ☐ Informal Number of Sheets _____
4. ☒ Oath or Declaration
- a. ☒ Newly executed (original or copy) ☐ Unexecuted
- b. ☐ Copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional application only)
- c. ☒ With Power of Attorney ☐ Without Power of Attorney
- d. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application,
see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference (usable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche (Appendix)
7. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all must be included)
- a. ☐ Paper Copy
- b. ☐ Computer Readable Copy (identical to computer copy)
- c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers (cover sheet & document(s))
9. ☐ 37 CFR 3.73(B) Statement (when there is an assignee)
10. ☐ English Translation Document (if applicable)
11. ☒ Information Disclosure Statement/PTO-1449 ☒ Copies of IDS Citations
12. ☒ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☐ Certificate of Mailing
- ☐ First Class ☐ Express Mail (Specify Label No.): _____

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Total Pages in this Submission

Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

Request That Application Not Be Published Pursuant To 35 U.S.C. 122(b)(2)

17. ☐ Pursuant to 35 U.S.C. 122(b)(2), Applicant hereby requests that this patent application not be published pursuant to 35 U.S.C. 122(b)(1). Applicant hereby certifies that the invention disclosed in this application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication of applications 18 months after filing of the application.

Warning

An applicant who makes a request not to publish, but who subsequently files in a foreign country or under a multilateral international agreement specified in 35 U.S.C. 122(b)(2)(B)(i), must notify the Director of such filing not later than 45 days after the date of the filing of such foreign or international application. A failure of the applicant to provide such notice within the prescribed period shall result in the application being regarded as abandoned, unless it is shown to the satisfaction of the Director that the delay in submitting the notice was unintentional.

UTILITY PATENT APPLICATION TRANSMITTAL
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XA-9375

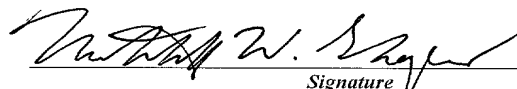
Total Pages in this Submission

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	23	- 20 =	3	x \$18.00	\$54.00
Indep. Claims	6	- 3 =	3	x \$80.00	\$240.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					\$0 00
BASIC FEE					\$710.00
OTHER FEE (specify purpose) Assignment Recordation Fee					\$40 00
TOTAL FILING FEE					\$1,044.00

- ☒ A check in the amount of **\$1,044.00** to cover the filing fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **22-0585** as described below. A duplicate copy of this sheet is enclosed.
- ☐ Charge the amount of _____ as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).


Signature

Reg. No. 31,568

Dated: October 12, 2000

Mitchell W. Shapiro
Vorys, Sater, Seymour & Pease LLP
1828 L Street, N.W.
Eleventh Floor
Washington, D.C. 20036
(202) 467-8812

CC:

5 program unit, based on execution priority information that
6 is given by some of the parameters.--

1 --23. The operating system according to claim 7,
2 wherein:

3 the allocating resources includes determining the
4 number of program units to be mapped for a specific page of
5 the cache memory, based on execution priority information
6 that is given by some of the parameters.

REMARKS

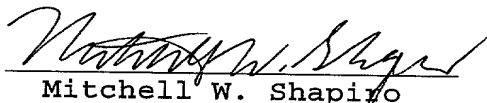
The purpose of this Preliminary Amendment is to eliminate the multiple dependent claims in order to avoid the fee for such claims.

The Commissioner is hereby authorized to charge to Deposit Account No. 22-0585 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

MWS:pdh

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October 12, 2000

By: 
Mitchell W. Shapiro
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SPECIFICATION

TITLE OF THE INVENTION

CACHE MEMORY ALLOCATION METHOD

FIELD OF THE INVENTION

The present invention relates to a method of allocating a cache memory included in a computer system, and moreover relates to an operating system having the capability of cache memory allocation and a computer system operating under the control of such operating system.

BACKGROUND OF THE INVENTION

With the advance of microprocessor hardware, it is now required that software operating on the hardware has more advanced capabilities correspondingly. As one of such capabilities, a "multiprocessing capability" for concurrent running of a plurality of software units on a single microprocessor unit is required even for small information processing devices such as personal computers.

As software for implementing the above capability, an operating system (OS) is prepared to take a duty of putting multiple running processes in order: the OS loads multiple processes in position into storage space and runs them in turn in a time-sharing manner. One of the roles of

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Another aspect of the advance of microprocessors is further increased processing speed. The most advanced microprocessors in current use have greater performance than large computers of about 15 years ago and image processing can be implemented by using a microprocessor, though it was impossible at that time.

A cache memory is a faster-access memory of small capacity to be used in addition to ordinary storage (main storage memory or simply, main storage). Access time for read/write of the cache memory is about five to ten times as fast as that of the main storage. On the other hand, the capacity of the main storage memory is 16M to 64M bytes for current standard personal computers, whereas the capacity of the cache memory is as small as 8K to 32K bytes.

Immediately after the power supply is turned on, the cache memory is empty. When program execution starts, the CPU reads instructions in the program one by one from the main storage and interprets and executes them, during which the read instructions are concurrently copied to the cache memory. If the cache memory becomes full, a suitable one of the previously copied instructions is erased and a new instruction is copied in place, in other words, overwrite is performed.

As far as the process described above be concerned, the use of the cache memory does not increase the processing speed. However, iteration of processing occurs during the execution of most programs, that is, a previously executed part of a program is executed again. When this happens, the CPU reads the copied instruction from the cache memory instead of accessing the main storage. As a result, the reading can be completed at a rate of five to ten times as fast as the rate of accessing the main storage. This effect becomes greater as the number of times of iteration occurring becomes larger.

In most fields of computer program application, relatively simple processing is often iterated many times during program execution. For example, in a computer

memory capacity is, for example, 8K bytes (2^{13} bytes, where symbol 2^* denotes exponentiation), each byte is assigned a 13-bit address in a range of binary digits from "0000000000000" to "1111111111111." On the other hand, addresses are assigned to main storage locations in the same way. If the main storage capacity is, for example, 32M bytes (2^{25} bytes), each byte is assigned a 25-bit address.

When the CPU copies an instruction to the cache memory, address signal lines of the main storage are used as is to determine the corresponding address in the cache memory. However, the cache memory capacity is smaller (the number of address signal lines is smaller), only the corresponding positions of the signal lines from the least significant bit (LSB) are used. For the memory of the above-mentioned capacity, an instruction stored at a main storage address, for example:

A = A24 A23 A22 ... A13 A12 A11 ... A2 A1
A0

(where each A_n contains a value of 0 or 1)
is copied to a cache memory address:

A = A12 A11 ... A2 A1 A0

This is expressed as a relation:

$A = A \bmod (2^{13})$ where mod denotes arithmetic giving modulo.

... [Equation 1]

In this method, any given main storage address A is converted into the corresponding cache memory address A' that is unique.

Only from the cache memory address A', even if being given solely, the corresponding main storage address from where the contents of the bits of the address A' have been copied cannot be determined because the bit positions A24 to A13 of the main storage address A from the most significant bit are unknown. Therefore, when an instruction is copied to the cache memory, the upper positions of the above address A:

$$A_t = A_{24} \quad A_{23} \quad A_{22} \quad \dots \quad A_{13}$$

are stored in the cache memory address A' together with the instruction. For this purpose, the cache memory is provided with auxiliary memory space for 12 bits (= 25 - 13) per byte. The above A_t portion is called a "tag" to the main storage address A.

A cache memory configuration discussed above is the simplest, but it is not effective because a 12-bit tag must be stored simultaneously for storing a 1-byte (8 bits) instruction in this configuration. As a modification to the above configuration, a line-configuration cache memory is prevailing. A line is a cache memory unit consisting of a plurality of bytes that are serial (for example, four bytes). Instruction copy and judgment of a hit/miss on the

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cache are executed on a line-by-line basis. In the line-configuration cache, a tag is stored for each line and therefore memory space can be saved. An address is assigned to each line and this address is called an entry address (or simply an entry) which differs from an ordinary address in meaning.

The same characteristics of cache memory as described above also apply to the line-configuration cache memory: i.e., the relation between a main storage address and the corresponding cache memory address (address per byte, not the entry address) is determined by [equation 1]; and the localized servicing of programs is a precondition for effective use of the cache memory.

Of course, not only instructions in a program but also data to be processed by a program may be copied to the cache memory without trouble.

As described above, the cache memory contributes toward enhancing the performance of a computer. Recently, it has been revealed that the cache memory, however, does not always function effectively in some case when the computer is used for multiprocessing.

The cache memory, as described in the previous section, is a performance-enhancing method applied on the assumption that programs (and data) are of localized servicing. On the other hand, multiprocessing is a

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time-sharing processing method for concurrent running of multiple programs. During the multiprocessing, thus, the CPU control for processing transfers to a different independent program after the elapse of a given period. Essentially, this has an adverse effect on the cache memory operation taking advantage of the localized servicing of programs. In fact, the cache memory is of no effect because, immediately after the transfer, the cache memory retains the contents of a program copied before the transfer and the CPU must read another program to which the control was transferred from the main storage. Thereafter, the cache memory would work effectively if iterative processing occurs (it is assumed that an individual program to be used is of localized servicing, causing a sufficient number of times of iterative processing). However, this is effective only before the next transfer of control occurs.

The occurrence of the above fact is particularly significant when the unit time (a time slice) of time sharing for multiprocessing is so short that iterative processing of a program is only possible by a limited number of times (five times, more or less) during the time slice. In this case, even if the access speed of the cache memory is ten times as fast as that of the main storage, the access speed for a complete time slice only increases by about three and a half times because the first time access must be performed

to the main storage. As compared with a case where iterative processing occurs a sufficient number of times and the access speed increases by about ten times, the short time slice causes the access speed to decrease by about one third.

The above phenomenon of performance decrease due to frequent occurrence of cache memory overwrite is called thrashing. To avoid thrashing, some measures for improvement have been proposed as will be described below, but any of these measures apparently have not produced a sufficient effect so far.

As a first measure for improvement, a method has been proposed in which the access to cache memory is granted to only a specific process (having execution priority) and other processes' instructions are not copied to the cache memory. In this method, the priority process can use the cache memory to advantage in the same way as a single process runs on the computer. However, this forces the CPU to run other processes at low performance without the cache memory.

As a second measure for improvement, a method has been proposed in which parallel cache memory units are provided to prevent contention between processes to use the cache. Specifically, a plurality of cache memory units (for example, two units) are installed on the computer system and instructions are copied to one of them that is empty. Judgment of a hit/miss on the cache, which is assumed two

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This method can avoid thrashing if the number of processes is equal to or less than the number of cache units. If, however, the number of processes is greater than the number of cache units, thrashing occurs as described above. In recent personal computer application, many processes (five or more) are executed simultaneously and there are many cases where each process is further divided into a plurality of sub-processes (threads), and consequently it is difficult to install a sufficient number of cache memory units on the computer so that these processes can be executed without contention. Even if a sufficient number of cache units are provided, a complexity of control circuits is required to control parallel operation of these units. To implement, for example, the above judgment of a hit/miss on the cache, after the comparison between a tag and the corresponding upper bits of main storage address is executed

for all cache units, a function of selecting a specific unit, according to the result of the comparison, is required. Especially for a miss on the cache, complicated calculation (LRU-algorithm) is required to determine a cache unit into which the instruction read from the main storage is overwritten and the processing time increases. Consequently, the thus increased processing time cancels out faster access that is a feature of the cache memory and the second method application to this case is not considered practical. CPUs that are now widely used for personal computers employ four cache units (called four ways) to eight cache units, the upper limit.

An object of the present invention is to provide a method of using the cache memory such that thrashing can be avoided with minimized hardware expansion, improving cache operation under the above circumstances.

Other objects of the present invention will be elucidated by the whole text of the present specification and the related drawings.

SUMMARY OF THE INVENTION

Typical implementations of the invention disclosed herein will be summarized below.

Allocation of resources available on a computer system to run a plurality of program units is carried out

by the following in combination: a step of receiving a request for running a program unit; a step of obtaining parameters that represent the attributes of the program unit; a step of allocating resources required to run the program unit, based on a resource allocation table and a cache management table as well as the above parameters; a step of registering results of allocating resources into the resource allocation table; and a step of registering an allocated storage domain of a cache memory to be used for the program unit into the cache management table.

Furthermore, specifically, the above parameters give positional information for a principal part to be executed at a high frequency in the program unit, the above resource allocation table has address reference information on a main storage to be used for program units, and the above cache management table lists addresses of the cache memory and program units mapped in cache address domains. The allocation of resources is implemented such that the above step of allocating resources determines an address of area to be used for the program unit in the main storage, ensuring that the principal part of the program unit is assigned an entry address of free cache area, based on the positional information for the principal part, the address reference information, and the cache management table.

General Information		Financial Data		Operational Data		Human Resources		Marketing Data	
Item	Value	Item	Value	Item	Value	Item	Value	Item	Value
Company Name	ABC Corporation	Revenue	\$1,200,000	Production Volume	150,000 units	Employees	50	Website	www.abc.com
Address	123 Main St, New York, NY 10001	Profit	\$200,000	Quality Score	95%	Managers	10	Phone	(212) 555-1234
City	New York	Expenses	\$1,000,000	Customer Satisfaction	88%	Engineers	20	Fax	(212) 555-5678
State	NY	Assets	\$500,000	Market Share	15%	Technicians	15	E-mail	info@abc.com
Zip	10001	Liabilities	\$300,000	Growth Rate	5%	Support Staff	5	URL	http://www.abc.com
Country	USA	Equity	\$200,000	Industry	Manufacturing	Quality Control	1	Product Line	Electronics
Industry	Manufacturing	Debt	\$100,000	Competitors	5	Inventory	10,000 units	Raw Materials	\$50,000
Market Segment	Consumer Goods	Current Ratio	1.67	Key Suppliers	3	Finished Goods	5,000 units	Manufacturing Costs	\$800,000
Product Line	Electronics	Debt to Equity Ratio	0.5	Distribution Channels	2	Warranty Claims	100	Logistics Costs	\$50,000
Key Suppliers	1	Return on Investment	16.7%	Logistics	1	Customer Support	24/7	Marketing Costs	\$30,000
Distribution Channels	2	Return on Assets	33.3%	Customer Support	24/7	Research & Development	\$100,000	Administrative Costs	\$20,000
Customer Support	24/7	Debt to Capitalization Ratio	0.33	Research & Development	\$100,000	Administrative Costs	\$20,000	Legal & Compliance	\$10,000
Research & Development	\$100,000	Current Ratio	1.67	Administrative Costs	\$20,000	Legal & Compliance	\$10,000	Insurance	\$5,000
Administrative Costs	\$20,000	Debt to Equity Ratio	0.5	Insurance	\$5,000	Other	\$5,000	Total	\$1,200,000
Legal & Compliance	\$10,000	Return on Investment	16.7%	Other	\$5,000	Total	\$1,200,000		
Insurance	\$5,000	Return on Assets	33.3%						
Other	\$5,000	Debt to Capitalization Ratio	0.33						
Total	\$1,200,000	Current Ratio	1.67						
		Debt to Equity Ratio	0.5						
		Return on Investment	16.7%						
		Return on Assets	33.3%						
		Debt to Capitalization Ratio	0.33						
		Current Ratio	1.67						
		Debt to Equity Ratio	0.5						
		Return on Investment	16.7%						
		Return on Assets	33.3%						
		Debt to Capitalization Ratio	0.33						
		Current Ratio	1.67						
		Debt to Equity Ratio	0.5						
		Return on Investment	16.7%						
		Return on Assets	33.3%						
		Debt to Capitalization Ratio	0.33						
		Current Ratio	1.67						
		Debt to Equity Ratio	0.5						
		Return on Investment	16.7%						
		Return on Assets	33.3%						
		Debt to Capitalization Ratio	0.33						
		Current Ratio	1.67						
		Debt to Equity Ratio	0.5						
		Return on Investment	16.7%						
		Return on Assets	33.3%						
		Debt to Capitalization Ratio	0.33						
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		Debt to Equity Ratio	0.5						
		Return on Investment	16.7%						
		Return on Assets	33.3%						
		Debt to Capitalization Ratio	0.33						
		Current Ratio	1.67						
		Debt to Equity Ratio	0.5						
		Return on Investment	16.7%						
		Return on Assets	33.3%						

[illegible][illegible]

By configuring a computer system to implement resource (specifically, cache) allocation as described above, the above-mentioned programs can be solved. A major source of thrashing is contention between multiple program units (processes or threads) to use the cache memory. It is apparent that some limitation is placed on avoiding the thrashing by hardware improvements, which have been taken conventionally. Therefore, the present invention offers a solution based on a cooperative system of software and hardware. That is, on the premise that the occurrence of contention for using the cache memory is inevitable as long as there are limitations on hardware expansion, the present invention provides preventive measures against significant thrashing developing by software-related contrivance.

Processing is greatly influenced by a miss on the cache if thrashing occurs when allocating the cache for a

Table 1. Demographic characteristics of the study population	
Age (years)	65.0 ± 10.0
Gender (male/female)	100/100
Education (years)	12.0 ± 2.0
Occupation (white/blue)	100/100
Marital status (married/divorced/widowed)	100/100/100
Income (USD/month)	1,000 ± 200
Health insurance (private/public)	100/100
Smoking status (smoker/non-smoker)	100/100
Alcohol consumption (yes/no)	100/100
Comorbidities (hypertension/diabetes/cholesterol)	100/100/100
Medication (antidepressant/antipsychotic)	100/100
Duration of illness (years)	10.0 ± 5.0
Previous hospitalizations (yes/no)	100/100
Family history of mental illness (yes/no)	100/100
Current living situation (alone/with family)	100/100
Stress levels (high/low)	100/100
Support system (strong/weak)	100/100
Quality of life (high/low)	100/100
Overall health status (good/poor)	100/100

Although the invention described above is effective when being applied independently, the invention is more effective when being combined with thrashing preventive measures provided for the hardware (such as dividing the cache memory into pages).

Other objects and advantages of the invention will become apparent during the following discussion of the accompanying drawings, wherein:

Fig. 2 is a block diagram showing the overall structure of a computer system on which the present invention is to be implemented;

Fig. 4 is a flowchart illustrating the operation of OS by an interrupt occurring from a timer;

Fig. 6 is a circuit diagram showing a second configuration of cache memory system (by an application space sharing scheme);

Fig. 7 is a circuit diagram showing a third configuration of cache memory system (by a cache page register scheme);

Fig. 8 shows the forms of a resource allocation table and a status retention table that are used by the OS to execute management of multiple concurrent processes;

Fig. 9 shows two forms of a cache management table; one for the first embodiment of the present invention and the other for a second or third embodiment of the invention;

Fig. 10 shows a form of the cache management table appropriate for a combination of the first embodiment and the second or third embodiment;

Fig. 11 shows forms of attribute information appropriate for the first embodiment of the present invention and the second or third embodiment of the invention;

Fig. 12 is a flowchart illustrating the operation of the means of resource allocation 999 in the second embodiment of the invention;

Fig. 13 is a flowchart illustrating the operation of the means of resource allocation 999 in the third embodiment of the invention; and

Fig. 14 is a flowchart illustrating an additional step of the OS operation in the third embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be explained below with reference to the drawings.

First, the overall structure of a computer system on which the present invention is to be implemented will be explained by using Fig. 2.

A computer system 10000 is configured in hardware with a CPU 1000 using a microprocessor, a ROM 1001, and a RAM 1002 that are interconnected by a bus 1003. In addition, an I/O channel 1004 is connected to the bus 1003, and through it, the following are connected to the above main portion of the system: a large-capacity auxiliary storage device 1005, an input device 1006 that is used for the operator to perform input operation, and a display device 1007 that visually informs the operator of the result of program execution. As the input device, a keyboard, a mouse, or a similar device is generally used. As the display device, a CRT display, a printer, or the like is generally used. As the auxiliary storage device 1005, a hard disk unit, a floppy disk unit, or the like is generally used.

A cache memory system 100 is provided in the CPU to achieve a higher rate of processing of the computer system. By using Fig. 5, an example of cache memory embodiment will be explained below.

Fig. 5 shows the hardware structure of a cache memory system for instructions, configured, according to a scheme called direct mapping, where the cache size is 8192 (8k) bytes and one line consists of four bytes (thus, the

The cache memory system 100 in the CPU 1000 has the following components:

An address selector circuit 101 receives an entry address input and selects a V-bit 111, tag 112, and line 113 that are designated by the entry address from among the

An address selector circuit 101 receives an entry address input and selects a V-bit 111, tag 112, and line 113 that are designated by the entry address from among the

V-bits 151, the tags 152, and the lines 153. The selected V-bit 111, tag 112, and line 113 are to be acted upon during further read/write operation of the cache memory system.

Other components of the cache memory system 100 are: a comparator circuit 103 for comparing tags, a hit signal 104 by which a hit/miss on the cache is judged, a byte selector 105 for selecting a desired byte out of a line, a cache fill counter 106 and an adder 107 that are used when a miss on the cache occurs, and an address selector 108 for selecting an address to be used by a byte selector 105. These components are connected as shown.

The above components of the cache memory operate as follows.

When the power supply to the system is turned on (or a system reset is performed), a reset signal 126 clears the V-bits in all entry addresses to 0 and the contents of the cache become invalid.

When the CPU 1000 attempts to execute an instruction in the main storage at address A that is specified by a program counter (PC) 1100, a check is performed to see whether the instruction has been copied to the cache memory in a location at an address corresponding to the address A. For this purpose, the 2nd to 12th bits of the PC, representing an entry address, are input to the address selector circuit 101 and a tag 112 and a V-bit 111 of the

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If the hit signal 104 is 0, it indicates a miss on the cache. In this case, it is necessary to fetch the instruction from the main storage and copy it to the cache (fill in the location of the cache with the instruction, which will be referred to as filling cache locations hereinafter). Because the procedure of filling cache locations does not influence the implementation of the present invention, its summary only will be described below.

Because the cache memory is composed of lines, when filling cache locations, a set of instructions to be stored per one line (four bytes) including the instruction at address A are copied into the locations of the cache memory, not only the single instruction at the address A. For this

In addition, a timer 1010 is connected to the CPU shown in Fig. 2 and activates an interrupt to the CPU at regular intervals (for example, 10 milliseconds) through a timer interrupt signal line 1011.

To control the operation of the computer system described above, software is prepared as will be describe below.

An operating system (OS) 200 is installed by being loaded into the ROM 1001 to control the operation of the present computer system as a whole, which is not always to be done in this way. The OS is capable of multiprocessing for parallel execution of multiple program units by time sharing, according to a method which will be described below, and includes means of resource allocation 999 for this multiprocessing. In the RAM, an OS area is reserved for the working area for the OS itself to operate and exclusively used by the OS. Of the hardware, the I/O channel 1004 and the auxiliary storage device 1005, the input device 1006, and the output device 1007 connected to the I/O channel are software controlled by the OS.

An interrupt routine address 201 that is the start address of an interrupt processing program within the OS is registered at a specific address in the ROM so that the OS executes predetermined operation in response to an interrupt signal from the timer. When the interrupt signal arrives at the CPU through the timer interrupt signal line 1011, a special circuit (not shown) for interruption in the CPU is activated and causes a jump to the interrupt routine address 201 by referring to this address.

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Application programs 221, 222, and so on are stored in the auxiliary storage device 1005 and copied to the RAM 1002 and run if necessary when requested by the operator. The application programs have their attribute information 231, 232, and so on that are required for running the programs and used by the OS. The contents of the attribute information are the size of the program, the start address of program execution, and the required working storage space in memory.

In the computer system described above, the OS operates as illustrated in Figs. 3 and 4.

Using the flowchart shown in Fig. 3, first, the following discusses the preparation of the OS when the power supply to the system is turned on (or a system reset is performed).

A disable interrupts instruction is issued (step 301, the simplified notation of s301 will be used hereinafter) to prevent an interrupt of the CPU from occurring before the completion of the OS preparation. Next, the storage areas for the following variables and tables are allocated in the OS area 210 and the variables and tables are initialized to predetermined initial values (s302 to s306). The storage area for variable N_proc that represents the number of processes is allocated and the N_proc variable is initialized to 0 (s302). The storage area

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for variable C_proc that represents the processing number being executed and the C_proc variable is initialized to 0 (s303).

Then, the storage area for a resource allocation table 700 whose form is shown in Fig. 8-a is allocated and the table is initialized (s304). Here, process number 0 is assumed to represent the OS itself. Next, the storage area for a status retention table 750 whose form is shown in Fig. 8-b is allocated (it is not necessary to initialize this table) (s305). Moreover, the storage area for a cache management table is allocated and the table is initialized (s306). The detail of this table will be described later.

When the above preparation has been completed, interrupts from the timer 1010 are enabled (s307) and the OS execution halts. Thereafter, the OS is activated each time an interrupt occurs.

Then, how the OS operates when an interrupt from the timer occurs will be explained below. A program to be called to execute this operation is stored in area following the interrupt routine address 201.

The operation of the OS to take place when an interrupt occurs is roughly divided into two: first operation is such that the OS runs a specific application program, according to the input from the operator; and second operation is process switching from the ongoing

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When an interrupt occurs, the OS first saves the current CPU status to save area 760 in the status retention table 750 (s311). This saving is executed so that the process that was running immediately before the interrupt occurring can restart in the same status after the completion of the OS operation. Although varying, depending on the type of the CPU, the following are to be saved: a value of PC 752 that indicates the address at which the running process stops by the interrupt, flag status 753 of the CPU, values of registers in the CPU, 754, 755, and so on.

For the first operation, the OS initially receives the entered name of the application program to run from the input device 1006 (s321). Then, the OS obtains the attribute information 231 for the program from the auxiliary storage device 1005 (s322). Using this information and taking the

contents of the above-mentioned tables into account, the OS activates the means of resource allocation 999 to allocate program area and working storage that are resources required to run the program (s323). Furthermore, the OS updates the resource allocation table, according to the allocation done (s324). After the completion of this update, the OS increments by one the N_proc variable that represents the number of processes (s325) and initializes the status retention table for this new process (s326) as follows. The PC value in this table is set at the start address from which the process run starts, that is, the sum of the content of program area start address 703 plus the value of entry address 902 (which will be described later) and other entry fields of the table are initialized to appropriate values (for example, 0).

Finally, the OS loads the program 221 into the main storage at an address determined by the s323 step. It is then possible to run the new process from its initial status next time its turn for run comes. Further processing is as will be done in the second operation that will be described below.

In the above description, the application programs 221, 222, and so on stored in the auxiliary storage device 1005 were assumed to run as single processes.

The OS first refers to the N_proc variable that represents the number of processes and its operation branches to any of the following (s331). If the N_proc variable is 0, the OS does nothing and halts its execution and then waits for the next interrupt. If the N_proc variable is 1, the OS makes the CPU restore to the same status as saved by retrieving the CPU status from the save area 760 (s332) and starts to run the process with the process number specified by the C_proc variable. If the N_proc variable is 2 or greater, the OS switches the ongoing process whose number is specified by the C_proc variable to the next numbered process by carrying out the following steps s333 to s337.

Then, the OS makes the CPU restore to the same status as saved in the status retention table for the process number

specified by the C_proc by retrieving the CPU status from this table (s337) and starts to run the process whose number is specified by the C_proc variable.

The performance of the OS in practical application would be more complex than as described above. For example, a same process may be run two times successively to allow priority execution of a specific process. If contention between multiple concurrent processes to get resources occurs (if, for example, a data file created by process A is used as the input to process B), adjustment is required to force one of the processes to wait. Furthermore, the input from the operator is not only the command to run an application program as illustrated above, but may be, for example, an input of a command to stop the ongoing process. The OS function to handle any possible command input is required. However, because the implementation of the present invention does not depend on the practical performance of the OS, further description of OS performance is not made herein.

In the above description, the cache management table 800 and the means of resource allocation 999 used in the s323 step can be made or configured in several ways, depending on the hardware configuration, which will be detailed in turn below.

As a first embodiment of the present invention, the "direct mapping" configuration of cache memory shown in Fig. 5 will first be discussed.

In this configuration, in order to prevent thrashing, it is advisable to position multiple concurrent processes on the main storage such that the principal parts of the processes do not use any same address on the cache memory. To do this, the following should be carried out: obtain the positions of the principal parts within the application programs from the attribute information 231, 232, and so on of the programs; determine the main storage addresses where the processes (programs) are to be loaded such that the corresponding cache addresses for storing the principal parts, which are determined by using the equation 1, differ from each other.

In this case, the required attribute information is provided in form shown in Fig. 11-a. That is, the attribute information 231 is recorded in this form, containing: program name 900, program size 901, entry address 902, working storage size 903, and in addition, address of principal part 910, and size of principal part 911. The entry address 902 and the address of principal part 910 are addressed in relative bytes from the beginning of the program.

Moreover, the cache management table retains information that each address domain of the cache memory is now occupied by what process or unoccupied in form shown in Fig. 9-a. That is, the cache management table 800 is a mapping table listing cache addresses 810 and process numbers 820 using the cache and mapped in cache address domains. If an address is unoccupied, the associated field of process number 820 contains a value of -1 indicating that no process exists in the address domain. When creating a cache management table (s306) during the preparation of OS, a value of 0 as the process number should be assigned for the address occupied by the OS and a value of -1 for all the remaining addresses. For simplifying purposes, the cache memory addressing domains in Fig. 9-a are fixed in units of 128 (\$80) bytes. However, organizing the cache management table 800 can be implemented in some other way; for example, the table may retain variable address domains appropriate for process numbers.

Using the above attribute information and cache management table as well as the above-mentioned resource allocation table 700, the means of resource allocation 999 operates, according to the flowchart shown in Fig. 1.

First, a new process number is set by adding one to the number of processes that are now running; i.e., $N_proc + 1$ (s2101). Further writing into the resource allocation

Seeking free area larger than the sum of program size 901 plus cache size (8KB) in the main storage is performed by using the resource allocation table 700 (s2105). The reason why the cache size (8KB) is added is that allowance is provided for shifting the address at which the program is loaded under a later step s2108.

Seeking free area larger than the size of principal part 911 in the cache memory is performed by using the cache management table 800 (s2106). In the cache address column 810 of the cache management table, the address domain from the start address of the free area thus found in the above step s2106 to the end address of the area containing the size of principal part is written. In the associated process number column 820, the process number $N_{proc} + 1$ is written

(s2107). Thereby, the cache memory storage for storing the principal part of the process is allocated.

Address L in the main storage at which the program is loaded is determined, according to the following equation (s2108):

$$L = (C - P - F) \bmod S + F \quad [\text{Equation 3}]$$

where C: Start address of the cache memory area found under s2106

P: Value of address of principal part 910

S: Size of cache memory

F: Start address of free main storage area found under s2105

By this step, the cache memory address domain to be used for the principal part of the program after the program is loaded agrees with the free cache memory area found under the step s2106.

The address L determined through the above step s2108, $L + \text{program size} - 1$, and $L + \text{entry address}$ are written into the columns 703, 704, and 705 of the resource allocation table, respectively (s2109). Thereby, the program area is allocated in the main storage.

The resources required for running the process have been reserved through the above steps, and then the operation of the means of resource allocation 999 terminates and the processing returns to the flowchart of Fig. 4-b.

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The components of the cache memory system in Fig. 6 and their operation are the same as those of the system in Fig. 5, but the difference between both lies in the way of generating an entry address. The system in Fig. 5 uses the 2nd to 12th bits of the value of the PC to generate an entry address, whereas the system in Fig. 6 uses the upper two bits (the 23rd and 24th bits) as is for the corresponding upper two bits of an entry address. Due to this, the bit positions from where the values are retrieved change, that is, the 11th to 22nd bits (12 bits in total) of the PC are used, though the number of bits of the tag 112 is unchanged. In the second embodiment, entry addresses are divided into four:

```
$000 to $1FF    ...    Page 0
$200 to $3FF    ...    Page 1
$400 to $5FF    ...    Page 2
$600 to $7FF    ...    Page 3
```


For the first embodiment in Fig. 5, the relationship between the main storage addresses and the corresponding cache memory addresses is expressed in the above-mentioned equation:

For the second embodiment, on the other hand, this relationship is expressed as follows:

..... [Equation 4]

The second term of [Equation 4], $\$200 \times (A \div \$800000)$, determines which cache page is to be used for the application program, according to the memory address assigned to the program. In other words, determining a memory (main storage) area to be allocated for an application program is, in effect, assigning a cache memory page to the application program.

In the configuration in Fig. 6, in order to prevent thrashing, it is advisable to position multiple concurrent processes on the main storage such that the processes use different cache memory pages. In this case, the information

Moreover, the cache management table retains information that each page of the cache memory is now occupied by what process or unoccupied in form shown in Fig. 9-b. That is, the cache management table 800 is a mapping table listing cache pages 811 and process numbers 820 using the cache and mapped in cache pages. If a page is unoccupied, the associated field of process number 820 contains a value of -1 indicating that no process exists on the page. When creating a cache management table (s306) during the preparation of OS, a value of 0 as the process number should be assigned for the page occupied by the OS and a value of -1 for all the remaining pages.

First, a new process number is set by adding one to the number of processes that are now running; i.e., `N_proc`

Program name 900 is written into the program name column 702 (s2202). Seeking free area larger than working storage size 903 in the main storage is performed by using the resource allocation table 700 (s2203). The start address of the thus found free area and the start address thereof plus the working storage size - 1 are written into the columns 706 and 707 of the resource allocation table, respectively (s2204). Thereby, the working storage is allocated in the main storage.

Furthermore, seeking free cache memory page is performed by using the cache management table 800 (s2205). In this table, in the process number column 820 associated with the page thus found under the above step s2250, the process number N_proc + 1 is written (s2206). Thereby, the cache memory page for the process is allocated.

$$L = C * (2^{*23}) \quad [\text{Equation 5}]$$

where C: Cache memory page number found under s2205

However, if one process occupies a plurality of cache pages, then this limits enhancing the processing rates

of other processes. When determining whether a plurality of cache pages is allocated for one process, the priority of the process must be considered. For priority consideration, required cache pages 920 (or equivalent priority information) should be registered in advance in the table of attribute information 231. It is advisable to apply the above equation 5' only if there are free cache pages and the process requires a plurality of pages.

In the above description, the size of one cache page has been assumed large enough to be allocated for only a single process at most. Consequently, the numbers of processes that can run concurrently are limited to the number of cache pages, which is not effective. Then, a method for improvement can be developed in combination of the second embodiment with the first embodiment as will be explained below.

Execution priority 930 is registered in advance in the table of attribute information 231 (Fig. 11-d). The execution priority is one of the following three levels:

Priority 3 (highest) The process exclusively uses a cache page.

Priority 2 (some priority) The process may share a cache page with other processes. However, the principal part of each process does not share a cache address domain with others.

Priority 1 (ordinary) The process may share a cache page with other processes. There is a possibility that the principal part of each process has the same cache address domain (a risk of thrashing is accepted).

The means of resource allocation 999 refers to the execution priority 930 and executes allocating a free cache page for a process of priority 3 in the method of second embodiment. For a process of priority 2, the means of resource allocation 999 selects a suitable cache page (but, not used for the process of priority 3) if there are no free cache pages and executes cache address domain allocation in the method of first embodiment. For a process of priority 1, the means of resource allocation 999 attempts the method of first embodiment, but loads the process for execution even if cache address domain allocation is impossible.

As the cache management table 800 for implementing the above method, the table shown in Fig. 10 is used. The table shown in Fig. 10, which is a combination of that shown in Fig. 9-a and that shown in Fig. 9-b, is a two-dimensional table consisting of cache page numbers 811 and cache address domains 810 on each page (relative addressing from the start address of page). In each column field 821 of the table, a process number that uses an address domain of a page is entered. A value of -1 indicates that the domain is unoccupied. An exclusive use field 830 for each page column

contains a value indicating whether a process exists that exclusively uses the page. If such process exists, the exclusive use field contains the process number thereof. Contained in the field, a value of -1 indicates that multiple concurrent processes share the page and a value of -2 indicates that the page is not used now at all. When this table is initialized (s306), all exclusive use fields 830 are initialized to -2 and all other fields are initialized to -1. Thereafter, the information for page and address domains used by the OS (process number 0) should be written into the table.

Furthermore, a third embodiment of the present invention will be explained below with reference to hardware configuration shown in Fig. 7. Fig. 7 shows an example of cache memory configuration based on a scheme called a "cache page register scheme," which is a modification to the cache memory configuration shown in Fig.5.

The components of the cache memory system in Fig. 7 and their operation are the same as those of the system in Fig. 5, but the difference between both lies in the way of generating an entry address. The system in Fig. 5 uses the 2nd to 12th bits of the value of the PC to generate an entry address, whereas the system in Fig. 7 is provided with a two-bit cache page register 160 and the contents of this register are used as upper two bits of an entry address. The

00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000

In the third embodiment, as is the case with the cache shown in Fig. 6, entry addresses are also divided into four:

Each page functions as an independent cache memory. Therefore, almost the same thrashing prevention measure as in the second embodiment applies to the third embodiment. Difference between the second and third embodiments lies in the following: change between cache pages automatically occurs, depending on the addressing of a process in the main storage for the cache shown in Fig. 6, whereas the OS must explicitly rewrite the contents of the cache page register in Fig. 7. That is, as shown in Fig. 14, after the step 337 in the process switching procedure in Fig. 4, an additional step (s338) of rewriting the cache page register 160 in accordance with the cache management table 800 is carried out.

Table 1. Demographic characteristics of the study population	
Age (years)	65.0 ± 10.0
Gender	
Male	50 (50.0%)
Female	50 (50.0%)
Education (years)	12.0 ± 2.0
Marital status	
Married	40 (80.0%)
Single	10 (20.0%)
Occupation	
Retired	30 (60.0%)
Unemployed	20 (40.0%)
Income (USD/month)	1000.0 ± 200.0
Health status	
Good	30 (60.0%)
Poor	20 (40.0%)
Comorbidities	
Hypertension	15 (30.0%)
Diabetes	10 (20.0%)
Cholesterol	12 (24.0%)
Arthritis	8 (16.0%)
Other	5 (10.0%)

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Married	40 (80.0%)
Single	10 (20.0%)
Occupation	
Retired	30 (60.0%)
Unemployed	20 (40.0%)
Income (USD/month)	1000.0 ± 200.0
Health status	
Good	30 (60.0%)
Poor	20 (40.0%)
Comorbidities	
Hypertension	15 (30.0%)
Diabetes	10 (20.0%)
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Marital status	
Married	40 (80.0%)
Single	10 (20.0%)
Occupation	
Retired	30 (60.0%)
Unemployed	20 (40.0%)
Income (USD/month)	1000.0 ± 200.0
Health status	
Good	30 (60.0%)
Poor	20 (40.0%)
Comorbidities	
Hypertension	15 (30.0%)
Diabetes	10 (20.0%)
Cholesterol	12 (24.0%)
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Marital status	
Married	40 (80.0%)
Single	10 (20.0%)
Occupation	
Retired	30 (60.0%)
Unemployed	20 (40.0%)
Income (USD/month)	1000.0 ± 200.0
Health status	
Good	30 (60.0%)
Poor	20 (40.0%)
Comorbidities	
Hypertension	15 (30.0%)
Diabetes	10 (20.0%)
Cholesterol	12 (24.0%)
Arthritis	8 (16.0%)
Other	5 (10.0%)

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Marital status	
Married	40 (80.0%)
Single	10 (20.0%)
Occupation	
Retired	30 (60.0%)
Unemployed	20 (40.0%)
Income (USD/month)	1000.0 ± 200.0
Health status	
Good	30 (60.0%)
Poor	20 (40.0%)
Comorbidities	
Hypertension	15 (30.0%)
Diabetes	10 (20.0%)
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Other	5 (10.0%)

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Marital status	
Married	40 (80.0%)
Single	10 (20.0%)
Occupation	
Retired	30 (60.0%)
Unemployed	20 (40.0%)
Income (USD/month)	1000.0 ± 200.0
Health status	
Good	30 (60.0%)
Poor	20 (40.0%)
Comorbidities	
Hypertension	15 (30.0%)
Diabetes	10 (20.0%)
Cholesterol	12 (24.0%)
Arthritis	8 (16.0%)
Other	5 (10.0%)

Although the foregoing discussed these embodiment models in which the present invention is applied as part of the OS functionality, it is possible to implement the present invention in such a manner that software developed to work as the embodiment models be added to an existing OS.

Although the invention has been described in its preferred form with a certain degree of particularity, it is understood that the present disclosure of the preferred form has been changed in the details of construction and the combination and arrangement of parts may be resorted to without departing from the spirit and the scope of the invention as hereinafter claimed.

WHAT IS CLAIMED IS:

1. Method of allocating resources available on a computer system to run a plurality of program units concurrently, comprising:

a step of receiving a request for running a program unit;

a step of obtaining parameters that represent the attributes of the program unit;

a step of allocating resources required to run the program unit, based on a resource allocation table and a cache management table as well as the parameters;

a step of registering results of the allocating resources into the resource allocation table; and

a step of registering an allocated storage domain of a cache memory to be used for the program unit into the cache management table.

2. The method of allocating resources according to claim 1, wherein:

the parameters give positional information for a principal part to be executed at a high frequency in the program unit;

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the step of allocating resources determines an address of area to be used for the program unit in the main storage, ensuring that the principal part of the program unit is assigned an entry address of free cache area, based on the positional information for the principal part, the address reference information, and the cache management table.

the step of allocating resources determines an address of area to be used for the program unit in the main

4. An operating system capable of running a plurality of program units concurrently:

- when receiving a request for running a new program unit, the operating system carrying out:
 - obtaining parameters that represent the attributes of the program unit;
 - allocating resources required to run the program unit, based on a resource allocation table and a cache management table as well as the parameters;
 - registering results of the allocating resources into the resource allocation table; and
 - registering an allocated storage domain of a cache memory to be used for the program unit into the cache management table.

5. The operating system according to claim 4,
wherein:
the cache memory has entry address domains, each of
which is specified by an entry address;
the parameters give positional information for a
principal part to be executed at a high frequency in the
program unit;

the resource allocation table has address reference information on a main storage to be used for program units;

the cache management table lists addresses of the cache memory and program units mapped in cache address domains; and

the allocating resources determines an address of area to be used for the program unit in the main storage, ensuring that an entry address to be assigned for the principal part to be executed at a high frequency in the program unit differs from an entry address assigned for any part to be executed at a high frequency in any program unit other than the program unit, based on the positional information for the principal part, the address reference information, and the contents of the cache management table.

6. The operating system according to claim 4, wherein:

the cache memory has a plurality of pages;

the resource allocation table has address reference information on a main storage to be used for program units;

the cache management table lists pages of the cache memory and program units mapped in cache pages; and

the allocating resources determines an address of area to be used for the program unit in the main storage, based on the positional information for the principal part,

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the address reference information, and the contents of the cache management table.

7. The operating system according to claim 6, wherein:

rewriting of a cache page register is performed, according to the contents of the cache management table, when the control of execution transfers from the program unit to another program unit.

8. The operating system according to claim 6 or 7, wherein:

the allocating resources includes determining the number of pages of the cache memory to be assigned for the program unit, based on execution priority information that is given by some of the parameters.

9. The operating system according to claim 6 or 7, wherein:

the allocating resources includes determining the number of program units to be mapped for a specific page of the cache memory, based on execution priority information that is given by some of the parameters.

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the resource allocation table has address reference information on a main storage to be used for program units;

the cache management table lists addresses of the cache memory and program units mapped in cache address domains; and

the allocating resources determines an address of area to be used for the program unit in the main storage, ensuring that an entry address to be assigned for the principal part to be executed at a high frequency in the program unit differs from an entry address assigned for any part to be executed at a high frequency in any program unit other than the program unit, based on the positional information for the principal part, the address reference information, and the contents of the cache management table.

12. The computer system according to claim 10, wherein:

the cache memory has a plurality of pages;

the resource allocation table has address reference information on a main storage to be used for program units;

the cache management table lists pages of the cache memory and program units mapped in cache pages; and

the allocating resources determines an address of area to be used for the program unit in the main storage, based on the address reference information and the contents of the cache management table as well as the parameters.

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13. A computer system including a CPU, a cache memory, and storage and running a plurality of program units concurrently:

the computer system having a resource allocation table into which results of allocating resources are registered and a cache management table into which allocated storage domains of the cache memory are registered;

the storage including an area for storing an operating system that controls the computer system; and

when running one of the plurality of program units, the operating system obtaining parameters for the program unit and allocating resources for the program unit, based on the contents of the resource allocation table and the cache management table as well as the parameters.

14. The computer system according to claim 13, wherein:

the cache memory has entry address domains, each of which is specified by an entry address;

the parameters give positional information for a principal part to be executed at a high frequency in the program unit;

the resource allocation table has address reference information on a main storage to be used for program units;

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the allocating resources determines an address of area to be used for the program unit in the main storage, ensuring that an entry address to be assigned for the principal part to be executed at a high frequency in the program unit differs from an entry address assigned for any part to be executed at a high frequency in any program unit other than the program unit, based on the positional information for the principal part, the address reference information, and the contents of the cache management table.

the cache memory has a plurality of pages;
the resource allocation table has address reference information on a main storage to be used for program units;
the cache management table lists pages of the cache memory and program units mapped in cache pages; and

the allocating resources determines an address of area to be used for the program unit in the main storage, based on the address reference information and the contents of the cache management table as well as the parameters.

when the computer system runs one of the plurality of program units, the operating system allocating resources for the program unit, ensuring that an entry address of a cache memory to be used for the principal part of the program unit differs from an entry address of the cache memory used for the principal part of one of the plurality of program units other than the program unit.

the allocating resources is executed by means of resource allocation included in the operating system.

the operating system has been stored into storage
of the computer system.

when running one of the plurality of program units, the computer system allocating resources for the program unit, based on the operating system, ensuring that an entry

address of a cache memory to be used for the principal part of the program unit differs from an entry address of the cache memory used for the principal part of one of the plurality of program units other than the program unit.

20. The computer system according to claim 19, wherein:

the allocating resources is executed by means of resource allocation that exists in the computer system.

21. The computer system according to claim 20, wherein:

the means of resource allocation is included in the operating system.

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ABSTRACT OF THE DISCLOSURE

To assure the multiprocessing performance of CPU on a microprocessor, the invention provides a method of memory mapping for multiple concurrent processes, thus minimizing cache thrashing. An OS maintains a management (mapping) table for controlling the cache occupancy status. When a process is activated, the OS receives from the process the positional information for a specific part (principal part) to be executed most frequently in the process and coordinates addressing of a storage area where the process is loaded by referring to the management table, ensuring that the cache address assigned for the principal part of the process differs from that for any other existing process. Taking cache memory capacity, configuration scheme, and process execution priority into account when executing the above coordination, a computer system is designed such that a highest priority process can have a first priority in using the cache.

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FIG. 1

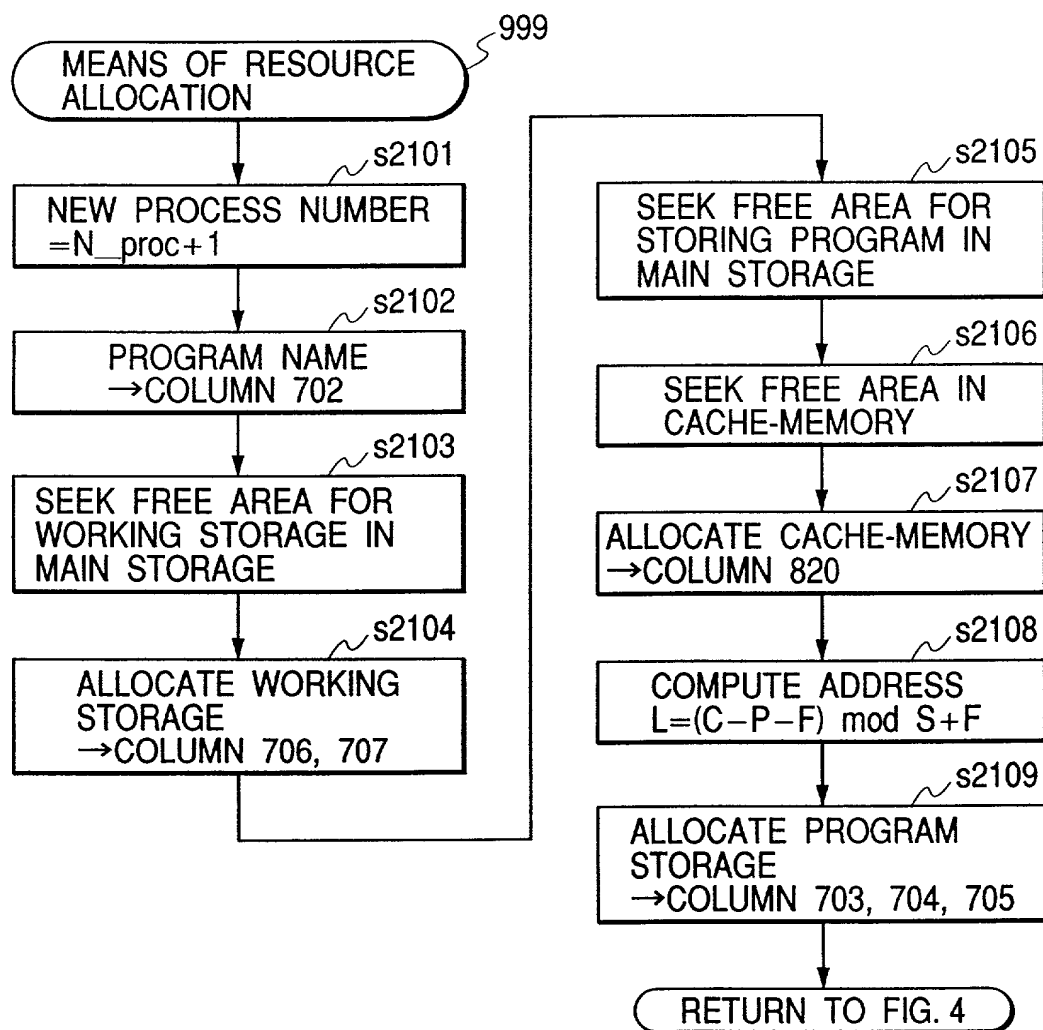


FIG. 2

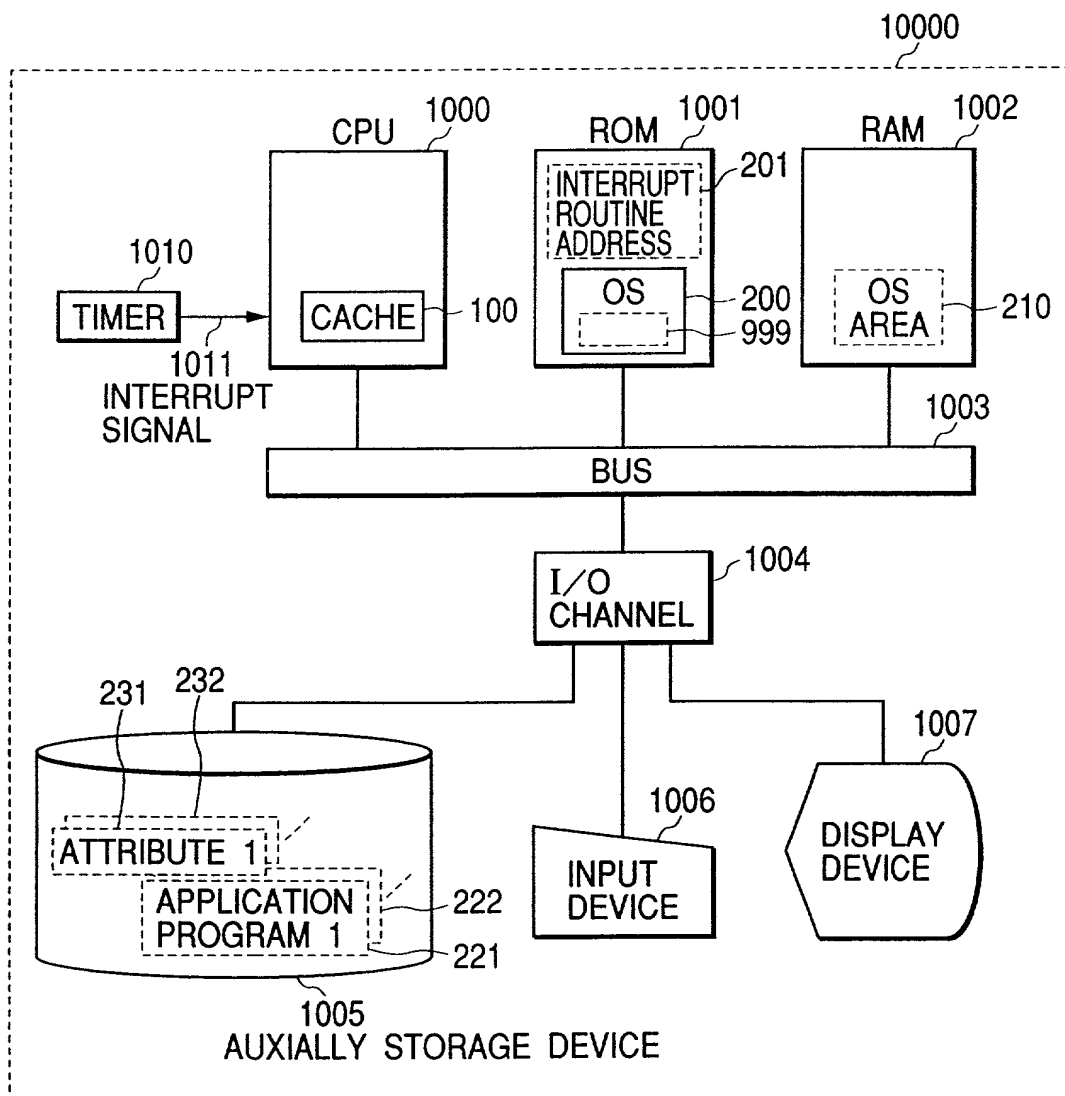


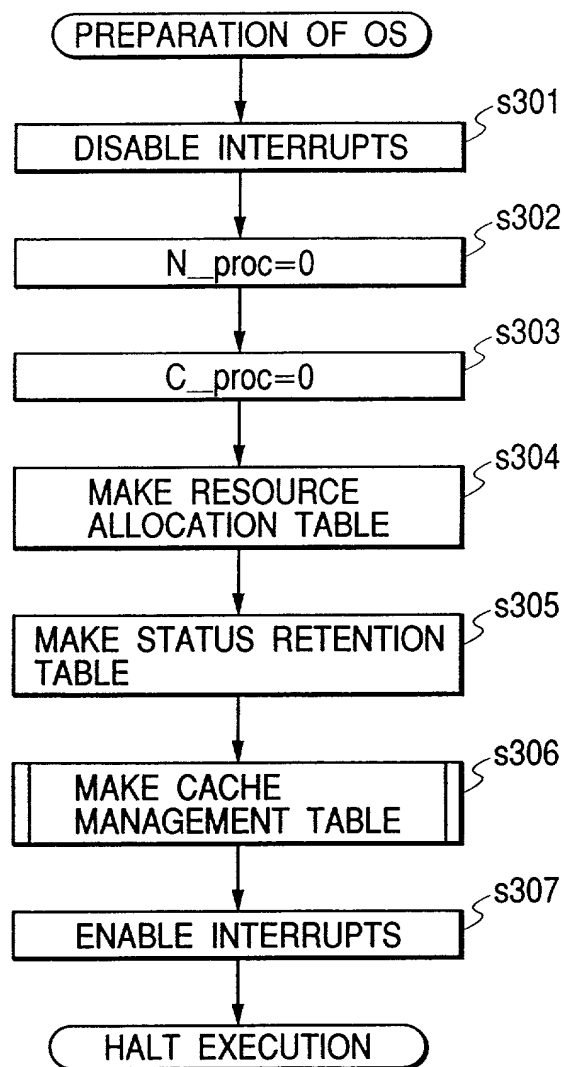
FIG. 3

FIG. 4

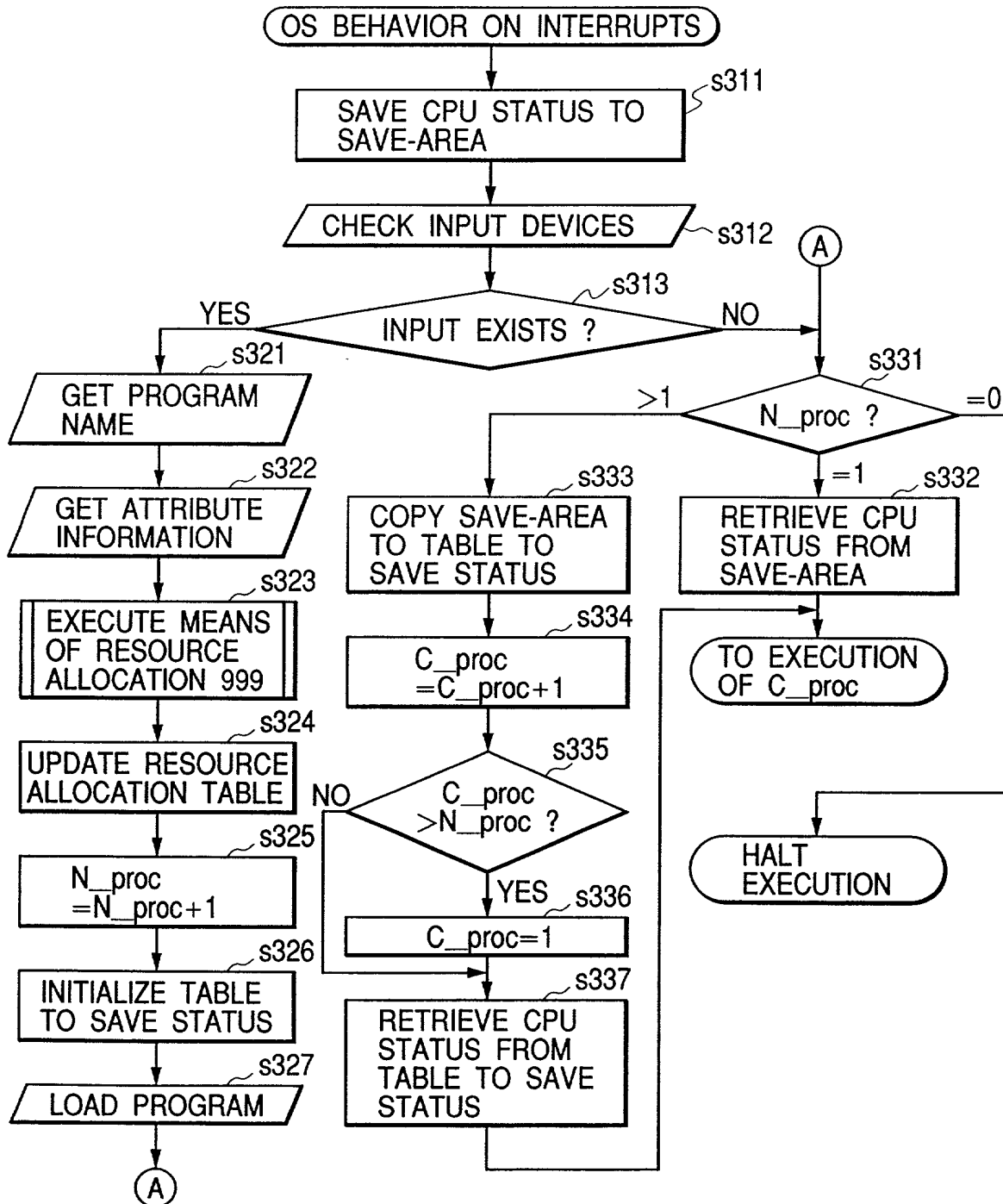
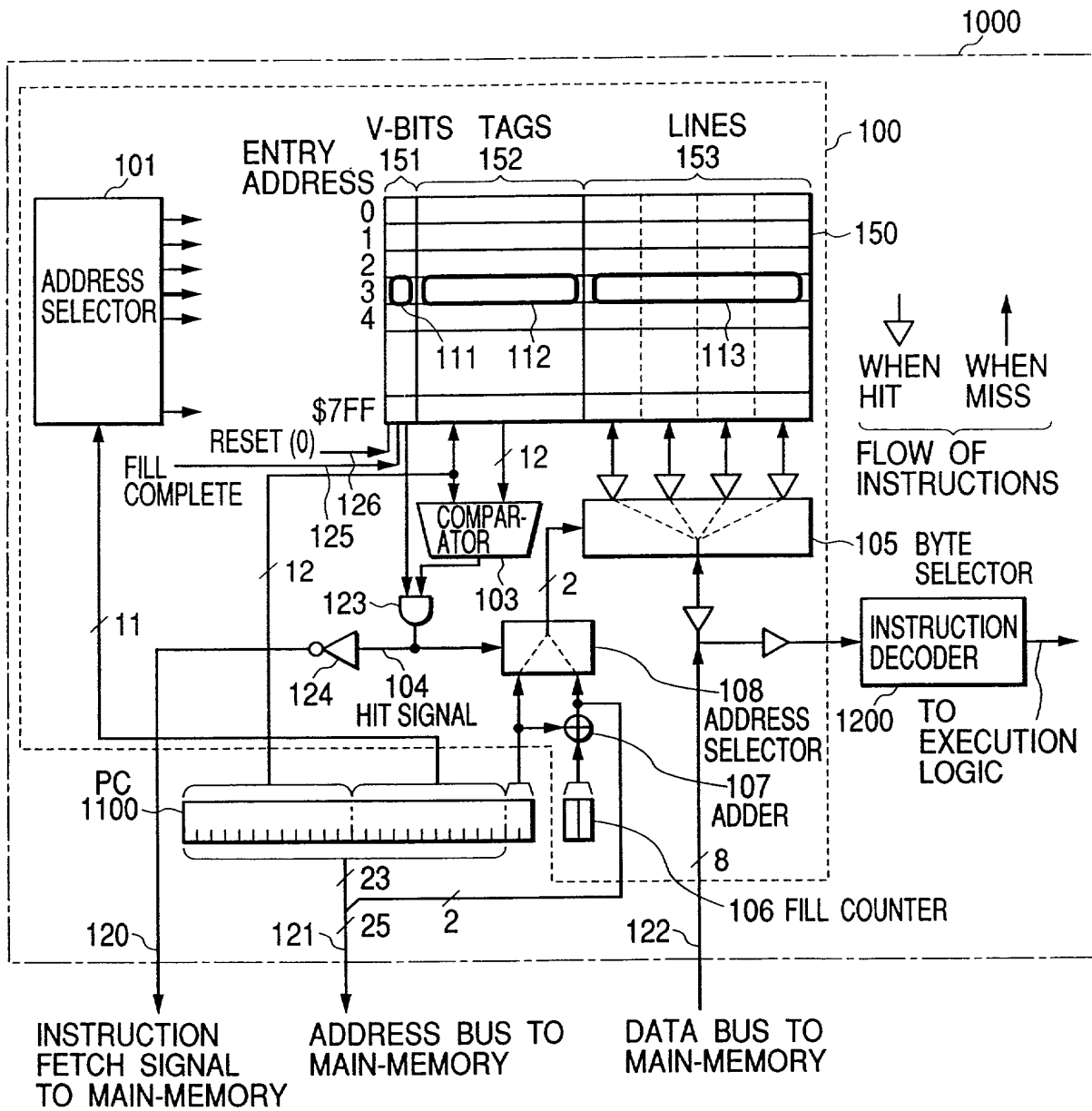


FIG. 5



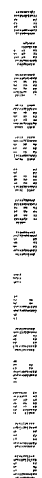
[illegible]

FIG. 7

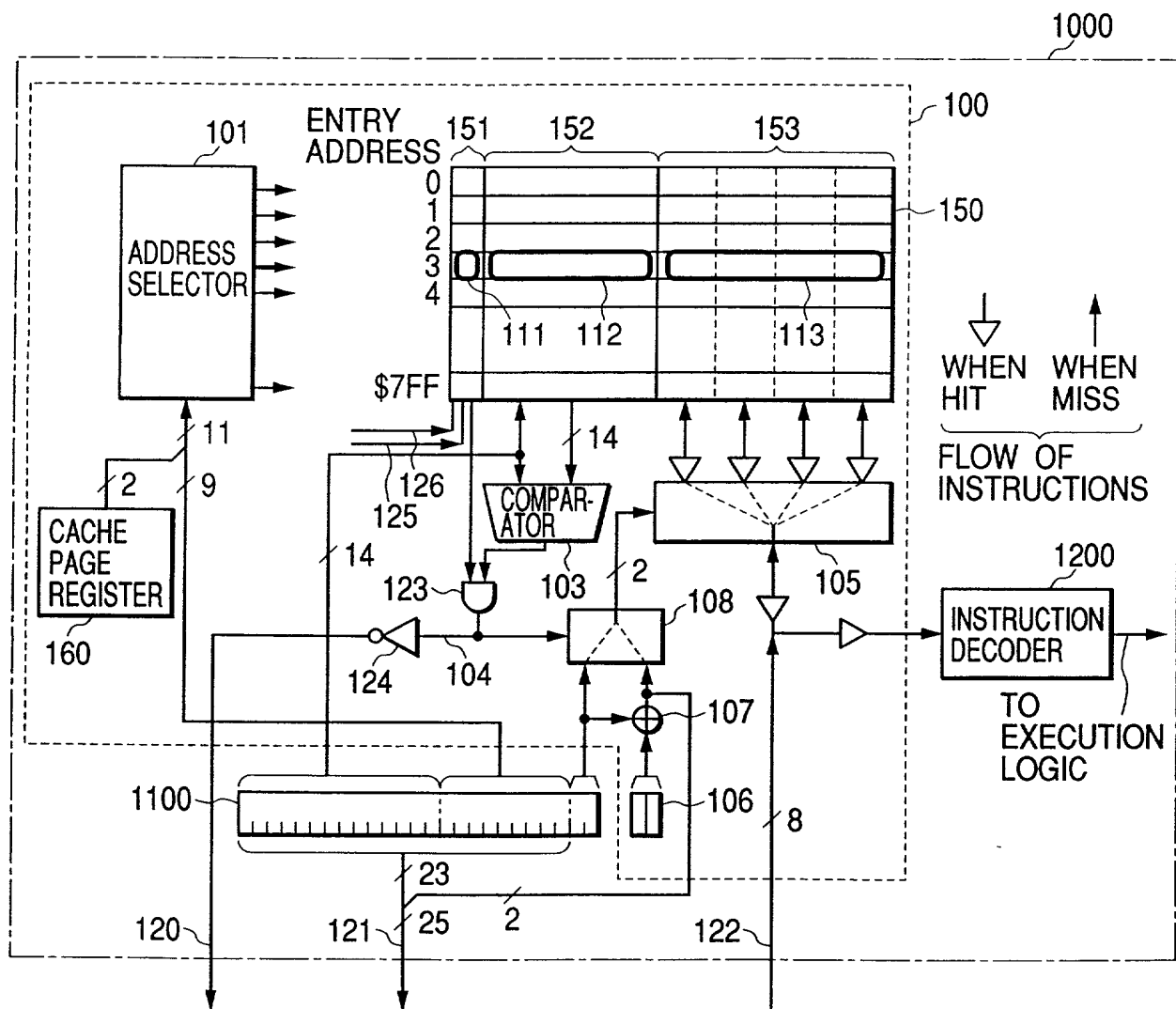


FIG. 8a

701	702	703	704	705	706	707
PROCESS NO.	PROGRAM NAME	PROGRAM AREA START ADDRESS	PROGRAM AREA END ADDRESS	EXECUTION ENTRY ADDRESS	WORKING STORAGE START ADDRESS	WORKING STORAGE END ADDRESS
0	OS	0	\$1FFFFFF	\$100000	\$200000	\$2FFFFFF
1						
2						
3						

FIG. 8b

751	752	753	754	755	
PROCESS NO.	PC	FLAG STATUS	REGISTER 1	REGISTER 2	
0 (OS)					760
1					
2					
3					
					770

FIG. 9a

810		820	
800		CACHE ADDRESS	PROCESS NO.
		\$000-\$07F	0
		\$080-\$0FF	0
		\$100-\$17F	1
		\$180-\$1FF	1
		\$200-\$27F	-1
		\$280-\$2FF	2
		\$300-\$37F	2
		\$380-\$3FF	2
		\$400-\$47F	-1
		\$480-\$4FF	-1
		\$500-\$57F	-1
		\$580-\$5FF	3
		\$1F00-\$1F7F	4
		\$1F80-\$1FFF	4

FIG. 9b

811		820	
800		CACHE PAGE	PROCESS NO.
		0	0
		1	-1
		2	-1
		3	-1

FIG. 10

800	CACHE ADDRESS \ CACHE PAGE	0	1	2	3	811
	EXCLUSIVE USE OF PAGE	0	-1	-1	-2	
	\$000-\$07F	0	1	3	-1	830
	\$080-\$0FF	0	1	3	-1	
	\$100-\$17F	0	1	3	-1	
	\$180-\$1FF	0	1	-1	-1	
	\$200-\$27F	0	-1	-1	-1	
	\$280-\$2FF	0	2	5	-1	
	\$300-\$37F	0	2	-1	-1	
	\$380-\$3FF	0	2	-1	-1	
	\$400-\$47F	0	-1	-1	-1	
						821
	\$700-\$77F	0	4		-1	810
	\$780-\$7FF	0	4		-1	

FIG. 11a

231

KIND OF ATTRIBUTE	VALUE
PROGRAM NAME	900
PROGRAM SIZE	901
ENTRY ADDRESS	902
ADDRESS OF PRINCIPAL PART	910
SIZE OF PRINCIPAL PART	911

FIG. 11b

231

KIND OF ATTRIBUTE	VALUE
PROGRAM NAME	900
PROGRAM SIZE	901
ENTRY ADDRESS	902

FIG. 11c

231

KIND OF ATTRIBUTE	VALUE
PROGRAM NAME	900
PROGRAM SIZE	901
ENTRY ADDRESS	902
ADDRESS OF PRINCIPAL PART	910
SIZE OF PRINCIPAL PART	911
REQUIRED CACHE PAGES	920

FIG. 11d

231

KIND OF ATTRIBUTE	VALUE
PROGRAM NAME	900
PROGRAM SIZE	901
ENTRY ADDRESS	902
ADDRESS OF PRINCIPAL PART	910
SIZE OF PRINCIPAL PART	911
EXECUTION PRIORITY	930

FIG. 12

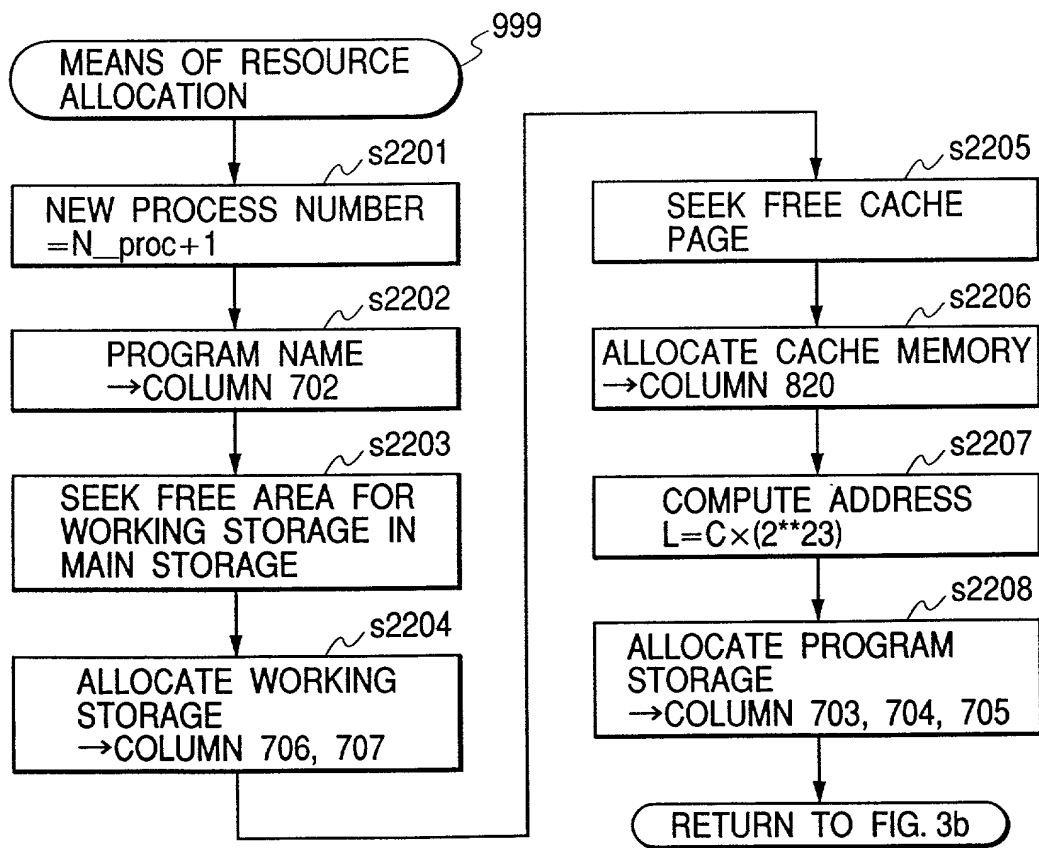
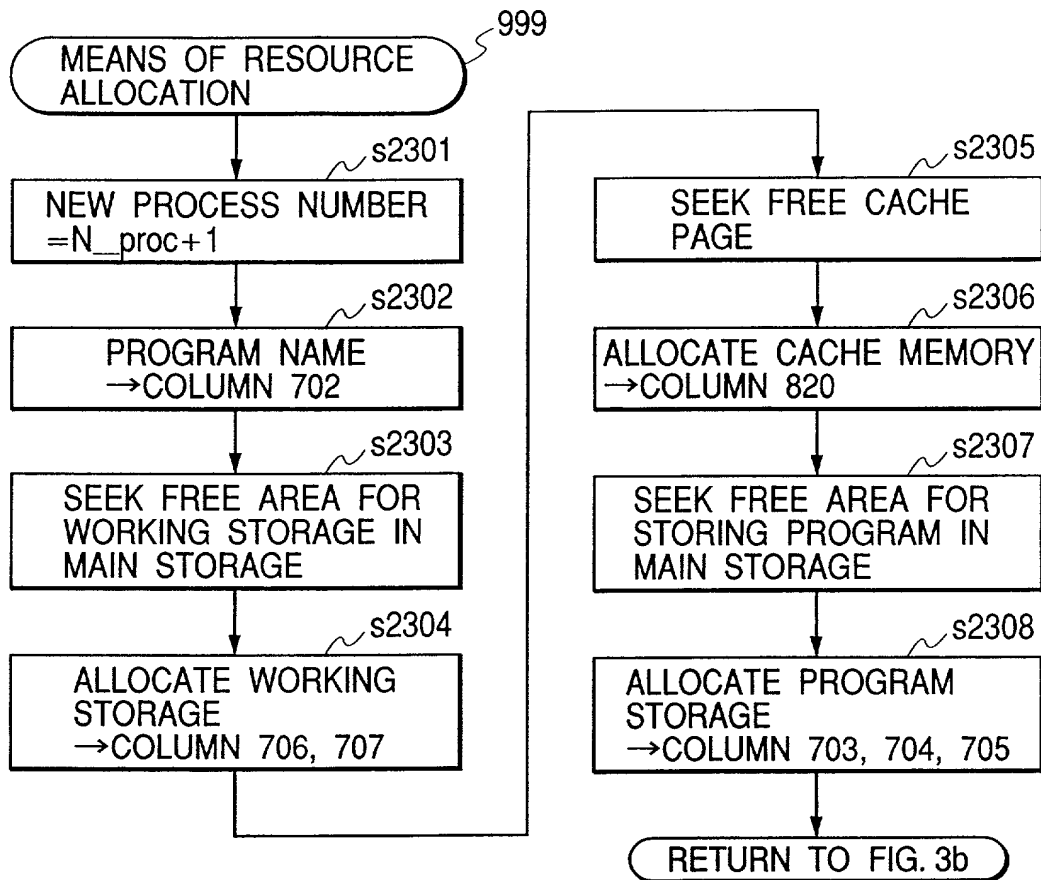
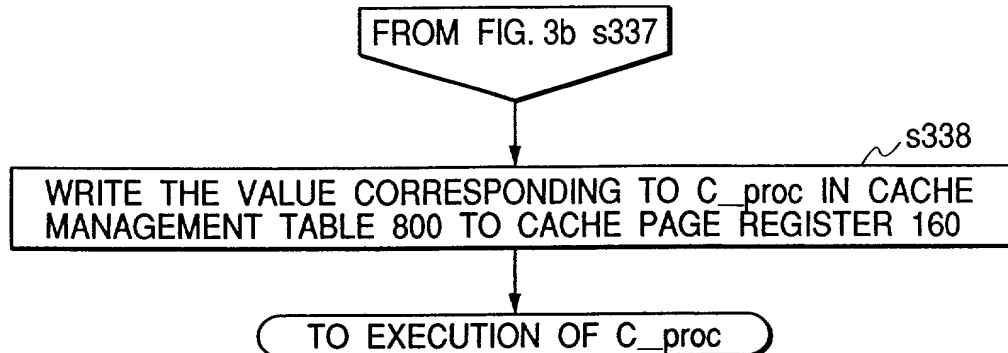


FIG. 13**FIG. 14**

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

CACHE MEMORY ALLOCATION METHOD

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

The specification of which is attached hereto unless the following box is checked:

☐ 月 日に提出され、米国出願番号または特許協定条約国際出願番号を _____ とし、
(該当する場合) _____ に訂正されました。

☐ was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されたとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

002207 09030960

Japanese Language Declaration (日本語宣言書)

私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基づき下記の、米国外の国の少なくとも一カ国を指定している特許協力条約365(a)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

Prior Foreign Application(s)

外国での先行出願

11-291807	Japan
(Number)	(Country)
(番号)	(国名)
(Number)	(Country)
(番号)	(国名)

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Priority Not Claimed

優先権主張なし

14/October/1999	<input type="checkbox"/>
(Day/Month/Year Filed)	
(出願年月日)	
	<input type="checkbox"/>
(Day/Month/Year Filed)	
(出願年月日)	

私は、第35編米国法典119条(e)項に基づいて下記の米国外特許出願規定に記載された権利をここに主張いたします。

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(Application No.)	(Filing Date)
(出願番号)	(出願日)

(Application No.)	(Filing Date)
(出願番号)	(出願日)

私は、下記の米国法典第35編120条に基づいて下記の米国外特許出願に記載された権利、又は米国外を指定している特許協力条約365条(c)に基づき権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国外特許出願に開示されていない限り、その先行米国外出願書提出日より以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

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(Application No.)	(Filing Date)
(出願番号)	(出願日)

(Status: Patented, Pending, Abandoned)	
(現況: 特許許可済、係属中、放棄済)	

(Application No.)	(Filing Date)
(出願番号)	(出願日)

(Status: Patented, Pending, Abandoned)	
(現況: 特許許可済、係属中、放棄済)	

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じているところに基づき表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Japanese Language Declaration

(日本語宣言書)

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POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (*list name and registration number*)

Nelson H. Shapiro, Reg. No. 17,095, Mitchell W. Shapiro,
Reg. No. 31,568, and the other practitioners associated
with the Customer Number 20,230

書類送付先

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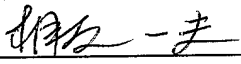
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Fax: (202) 467-8900

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発明者の署名	日付	Inventor's signature Date  9/20/2000
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国籍	Citizenship Japan	
私書箱	Post Office Address c/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan	

(第二以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for second and subsequent joint inventors.)

第二共同発明者名		Full name of second joint inventor, if any Keisuke TOYAMA	
第二共同発明者の署名	日付	Second inventor's signature	Date
		山 圭介	9/21/2000
住所		Residence Hodogaya, Japan	
国籍		Citizenship Japan	
私書箱		Post Office Address c/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan	
第三共同発明者名		Full name of third joint inventor, if any	
第三共同発明者の署名	日付	Third inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第四共同発明者名		Full name of fourth joint inventor, if any	
第四共同発明者の署名	日付	Fourth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	
第五共同発明者名		Full name of fifth joint inventor, if any	
第五共同発明者の署名	日付	Fifth inventor's signature	Date
住所		Residence	
国籍		Citizenship	
私書箱		Post Office Address	